National Semiconductor

March 14, 2008

LMP7721
3 Femtoampere Input Bias Current Precision Amplifier

General Description

The LMP7721 is the industry's lowest guaranteed input bias current precision amplifier. The ultra low input bias current is 3 fA, with a guaranteed limit of ±20 fA at 25°C and ±900 fA at 85°C. This is achieved with the latest patent pending technology of input bias current cancellation amplifier circuitry. This technology also maintains the ultra low input bias current over the entire input common mode voltage range of the amplifier.

Other outstanding features, such as low voltage noise (6.5 nV/$\sqrt{\text{Hz}}$), low DC offset voltage (±150 µV maximum at 25°C) and low offset voltage temperature coefficient (–1.5 µV/°C), improve system sensitivity and accuracy in high precision applications. With a supply voltage range of 1.8V to 5.5V, the LMP7721 is the ideal choice for battery operated portable applications. The LMP7721 is part of the LMP® precision amplifier family.

As part of National's PowerWise® products, the LMP7721 provides the remarkably wide gain bandwidth product (GBW) of 17 MHz while consuming only 1.3 mA of current. This wide GBW along with the high open loop gain of 120 dB enables accurate signal conditioning. With these specifications, the LMP7721 has the performance to excel in a wide variety of applications such as electrochemical cell amplifiers and sensor interface circuits.

The LMP7721 is offered in an 8-pin SOIC package with a special pinout that isolates the amplifier's input from the power supply and output pins. With proper board layout techniques, the unique pinout of the LMP7721 will prevent PCB leakage current from reaching the input pins. Thus system error will be further reduced.

Features

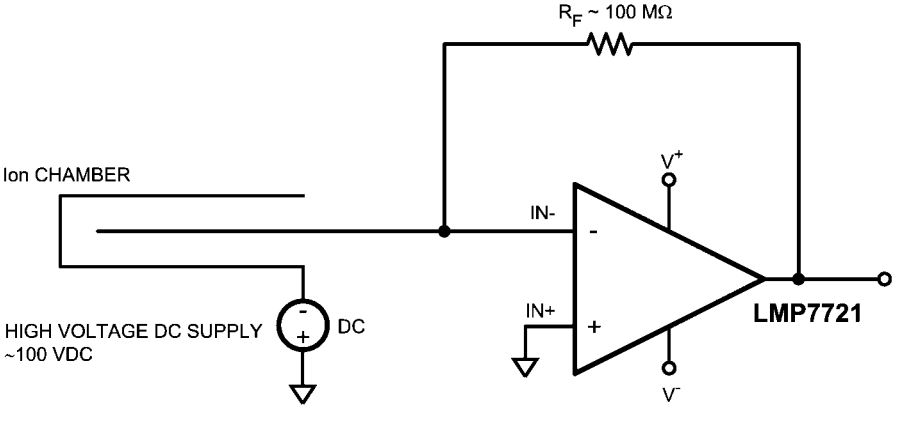
Unless otherwise noted, typical values at T_A = 25°C, V_S = 5V.

- Input bias current (V_{CM} = 1V)
  - — max @ 25°C ±20 fA
  - — max @ 85°C ±900 fA
- Offset voltage ±26 µV
- Offset voltage drift −1.5 µV/°C
- DC Open loop gain 120 dB
- DC CMRR 100 dB
- Input voltage noise (at f = 1 kHz) 6.5 nV/√Hz
- THD 0.0007%
- Supply current 1.3 mA
- GBW 17 MHz
- Slew rate (falling edge) 12.76 V/µs
- Supply voltage 1.8V to 5.5V
- Operating temperature range –40°C to 125°C
- 8-Pin SOIC

Applications

- Photodiode amplifier
- High impedance sensor amplifier
- Ion chamber amplifier
- Electrometer amplifier
- pH electrode amplifier
- Transimpedance amplifier

Block Diagram of a Typical Application



Ion Chamber: Current to Voltage Converter

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PowerWise® is a registered trademark of National Semiconductor.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2000V
Machine Model	200V
V_{IN} Differential	±0.3V
Supply Voltage ($V_S = V^+ - V^-$) (Note 10)	6.0V
Voltage on Input/Output Pins	V^+ +0.3V, V^- −0.3V
Storage Temperature Range	−65°C to 150°C
Junction Temperature (Note 3)	+150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering Lead Temp. (10 sec)	260°C

Operating Ratings (Note 1)

Temperature Range (Note 3)	−40°C to 125°C
Supply Voltage ($V_S = V^+ - V^-$)	
0°C ≤ T_A ≤ 125°C	1.8V to 5.5V
−40°C ≤ T_A ≤ 125°C	2.0V to 5.5V
Package Thermal Resistance (θ_{JA}(Note 3))	
8-Pin SOIC	190°C/W

2.5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V^+ = 2.5V, V^- = 0V, $V_{CM} = (V^+ + V^-)/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage				±50	±180 **±480**	µV
TC V_{OS}	Input Offset Voltage Drift (Note 6)				−1.5	−4	µV/°C
I_{BIAS}	Input Bias Current	V_{CM} = 1V (Notes 7, 8)	25°C		±3	±20	fA
			−40°C to 85°C			±900	
			−40°C to 125°C			**±5**	pA
I_{OS}	Input Offset Current	V_{CM} = 1V (Note 8)			6	40	fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.4V		83 **80**	100		dB
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5.5V V^- = 0V, V_{CM} = 0		84 **80**	92		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB		−0.3 **−0.3**		1.5 **1.5**	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.15V to 2.2V R_L = 2 kΩ to V^+/2		88 **82**	107		dB
		V_O = 0.15V to 2.2V R_L = 10 kΩ to V^+/2		92 **88**	120		
V_O	Output Swing High	R_L = 2 kΩ to V^+/2		70 **77**	25		mV from V^+
		R_L = 10 kΩ to V^+/2		60 **66**	20		
	Output Swing Low	R_L = 2 kΩ to V^+/2			30	70 **73**	mV
		R_L = 10 kΩ to V^+/2			15	60 **62**	
I_O	Output Short Circuit Current	Sourcing to V^- V_{IN} = 200 mV (Note 9)		36 **30**	46		mA
		Sinking to V^+ V_{IN} = −200 mV (Note 9)		7.5 **5.0**	15		
I_S	Supply Current				1.1	1.5 **1.75**	mA
SR	Slew Rate	A_V = +1, Rising (10% to 90%)			9.3		V/µs
		A_V = +1, Falling (90% to 10%)			10.8		

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
GBW	Gain Bandwidth Product			15		MHz
e_n	Input-Referred Voltage Noise	f = 400 Hz		8		$nV/\sqrt{Hz}$
		f = 1 kHz		7		
i_n	Input-Referred Current Noise	f = 1 kHz		0.01		$pA/\sqrt{Hz}$
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 2, R_L = 100 kΩ V_O = 0.9 V_{PP}		0.003		%
		f = 1 kHz, A_V = 2, R_L = 600Ω V_O = 0.9 V_{PP}		0.003		

5V Electrical Characteristics

Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V+ = 5V, V− = 0V, V_{CM} = (V+ + V−)/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage				±26	±150 **±450**	µV
TC V_{OS}	Input Offset Average Drift (Note 6)				−1.5	−4	µV/°C
I_{BIAS}	Input Bias Current	V_{CM} = 1V (Notes 7, 8)	25°C		±3	±20	fA
			−40°C to 85°C			±900	
			−40°C to 125°C			**±5**	pA
I_{OS}	Input Offset Current	(Note 8)			6	40	fA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.7V		84 **82**	100		dB
PSRR	Power Supply Rejection Ratio	1.8V ≤ V+ ≤ 5.5V V− = 0V, V_{CM} = 0		84 **80**	96		dB
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 80 dB CMRR ≥ 78 dB		−0.3 **−0.3**		4 **4**	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.3V to 4.7V R_L = 2 kΩ to V+/2		88 **82**	111		dB
		V_O = 0.3V to 4.7V R_L = 10 kΩ to V+/2		92 **88**	120		
V_O	Output Swing High	R_L = 2 kΩ to V+/2		70 **77**	30		mV from V+
		R_L = 10 kΩ to V+/2		60 **66**	20		
	Output Swing Low	R_L = 2 kΩ to V+/2			31	70 **73**	mV
		R_L = 10 kΩ to V+/2			20	60 **62**	
I_O	Output Short Circuit Current	Sourcing to V− V_{IN} = 200 mV (Note 9)		46 **38**	60		mA
		Sinking to V+ V_{IN} = −200 mV (Note 9)		10.5 **6.5**	22		
I_S	Supply Current				1.3	1.7 **1.95**	mA
SR	Slew Rate	A_V = +1, Rising (10% to 90%)			10.43		V/µs
		A_V = +1, Falling (90% to 10%)			12.76		
GBW	Gain Bandwidth Product				17		MHz

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
e_n	Input-Referred Voltage Noise	f = 400 Hz		7.5		$nV/\sqrt{Hz}$
		f = 1 kHz		6.5		
i_n	Input-Referred Current Noise	f = 1 kHz		0.01		$pA/\sqrt{Hz}$
THD+N	Total Harmonic Distortion + Noise	f = 1 kHz, A_V = 2, R_L = 100 kΩ V_O = 4 V_{PP}		0.0007		%
		f = 1 kHz, A_V = 2, R_L = 600Ω V_O = 4 V_{PP}		0.0007		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics Tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC) Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 4: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

Note 5: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlations using the Statistical Quality Control (SQC) method.

Note 6: Offset voltage average drift is determined by dividing the change in V_{OS} at the temperature extremes by the total temperature change.

Note 7: Positive current corresponds to current flowing into the device.

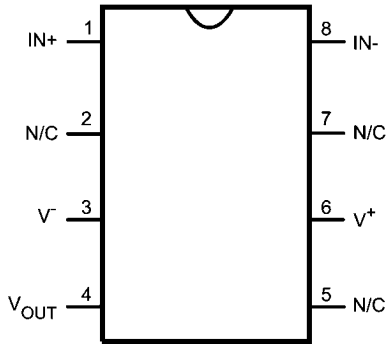
Note 8: This parameter is guaranteed by design and/or characterization and is not tested in production.

Note 9: The short circuit test is a momentary open loop test.

Note 10: The voltage on any pin should not exceed 6V relative to any other pins.

Connection Diagram

8-Pin SOIC



Top View

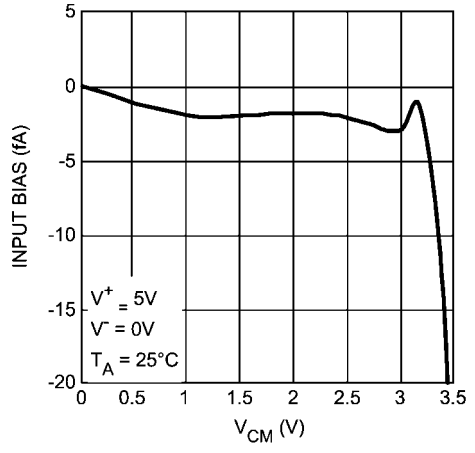
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMP7721MA	LMP7721MA	95 Units/Rail	M08A
	LMP7721MAX		2.5k Units Tape and Reel	

Typical Performance Characteristics

Unless otherwise specified: T_A = 25°C, V_{CM} = (V^+ + V^-)/2.

Input Bias Current vs. V_{CM}



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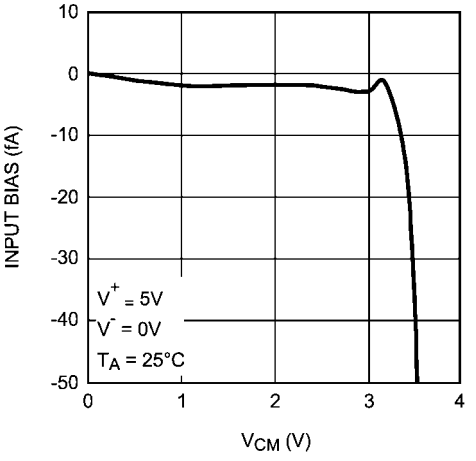
Input Bias Current vs. V_{CM}



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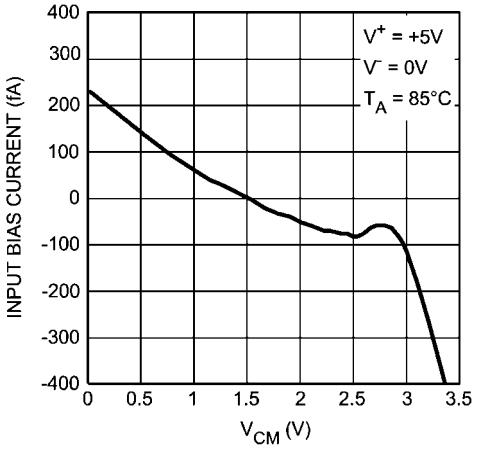
Input Bias Current vs. V_{CM}



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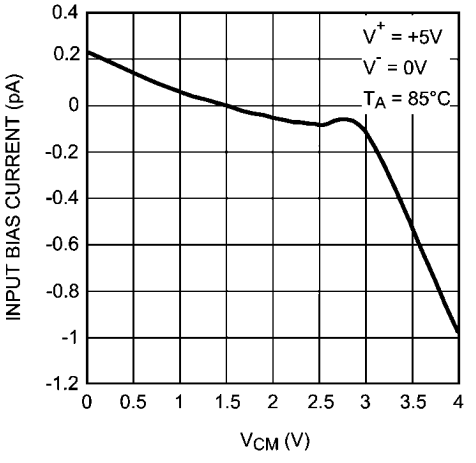
Input Bias Current vs. V_{CM}



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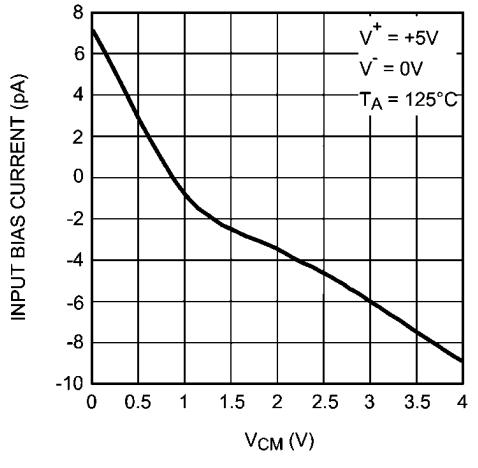
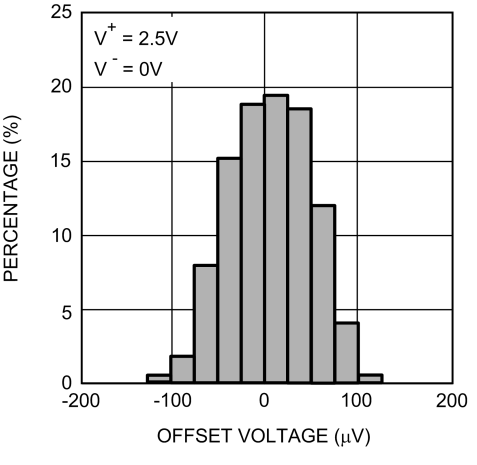
Input Bias Current vs. V_{CM}



20204085

Offset Voltage Distribution



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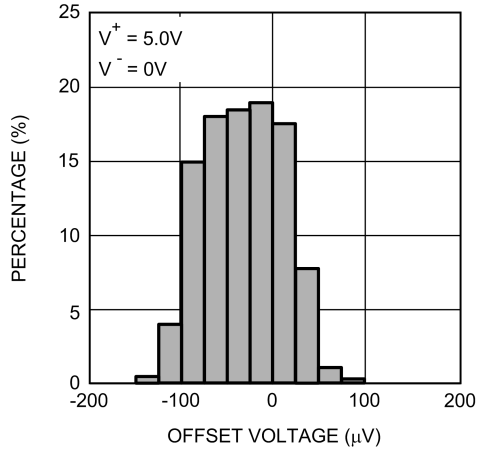
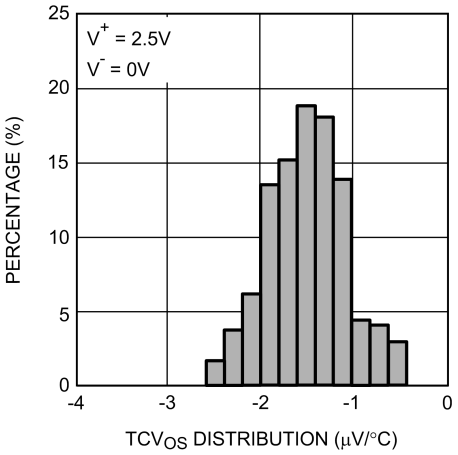
Offset Voltage Distribution



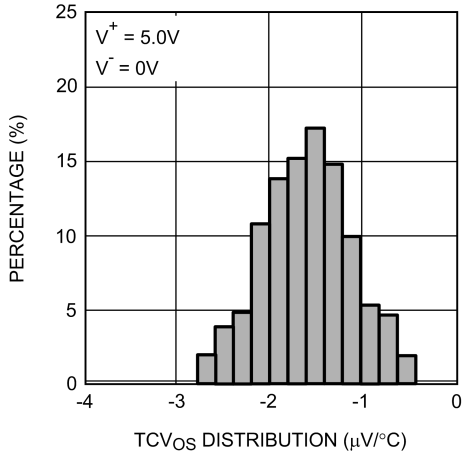
20204040

TCV_{OS} Distribution



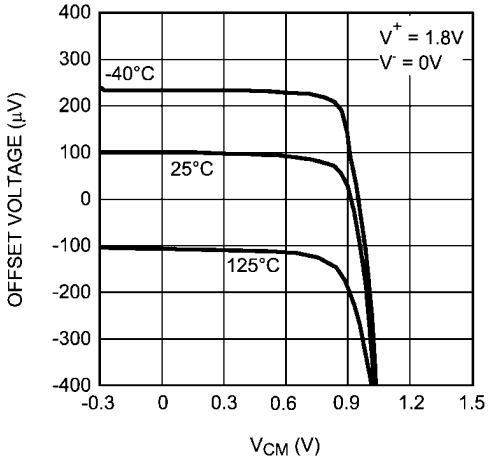
20204045

TCV_{OS} Distribution



20204046

Offset Voltage vs. V_{CM}



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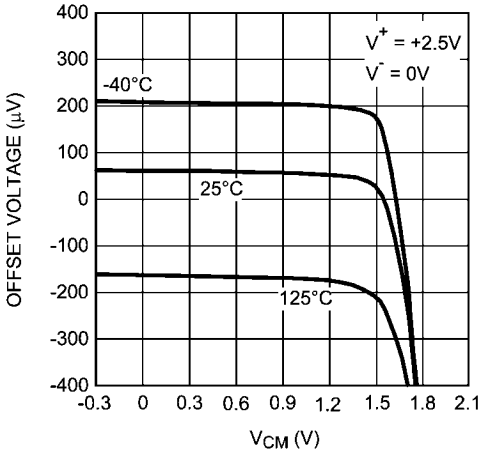
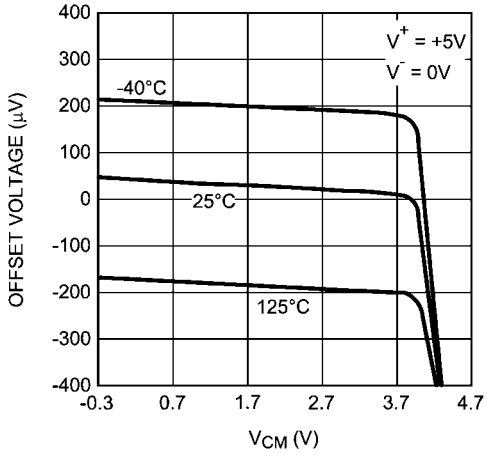
Offset Voltage vs. V_{CM}



20204022

Offset Voltage vs. V_{CM}



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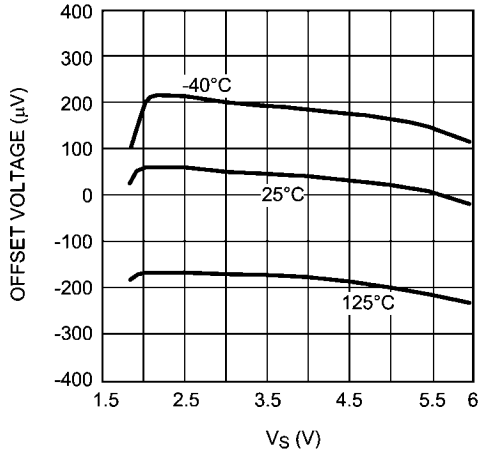
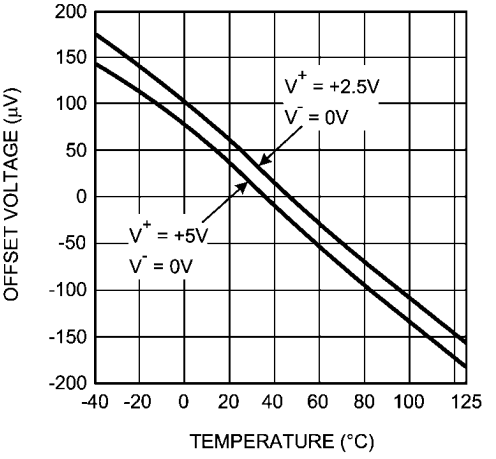
Offset Voltage vs. Supply Voltage



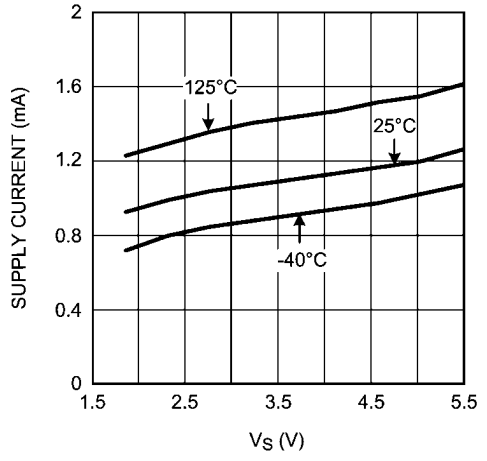
20204019

Offset Voltage vs. Temperature



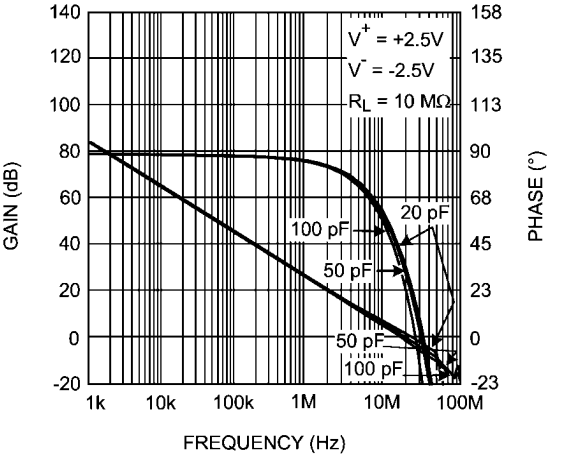
20204018

Supply Current vs. Supply Voltage



20204038

Open Loop Frequency Response Gain and Phase



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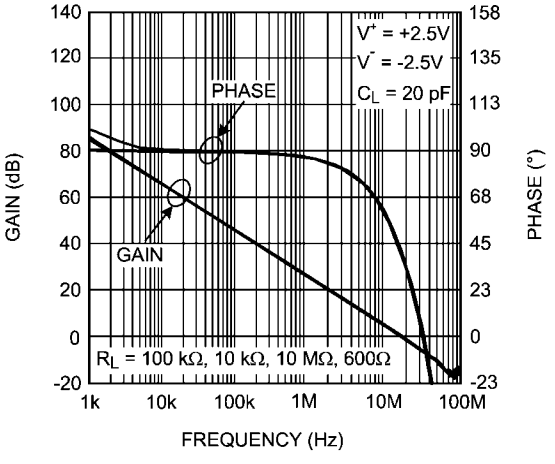
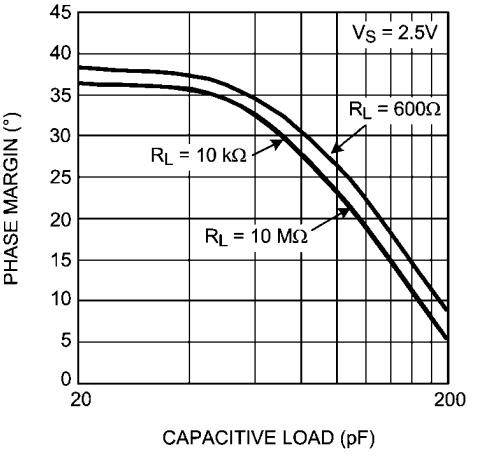
Open Loop Frequency Response Gain and Phase



20204014

Phase Margin vs. Capacitive Load



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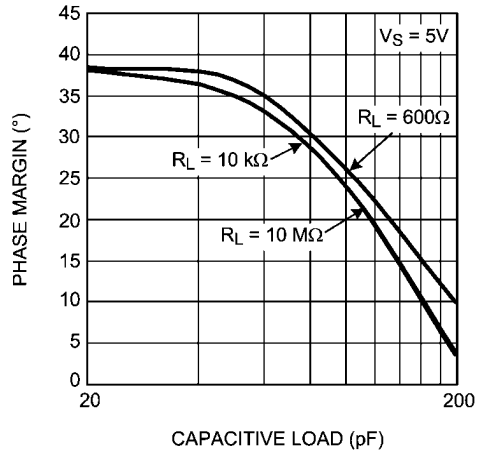
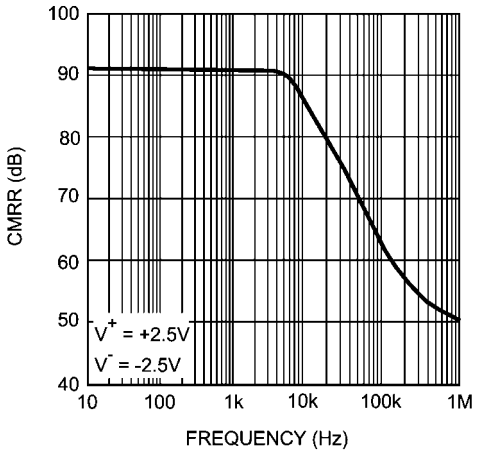
Phase Margin vs. Capacitive Load



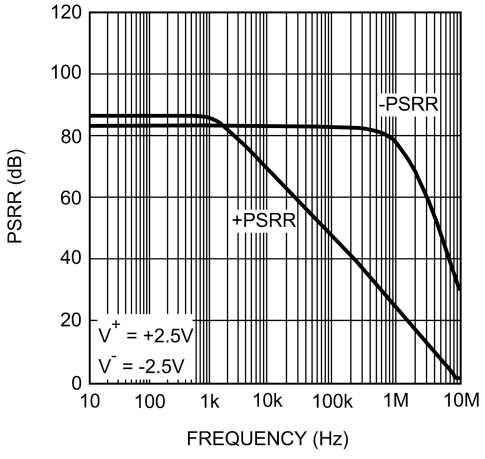
20204016

CMRR vs. Frequency



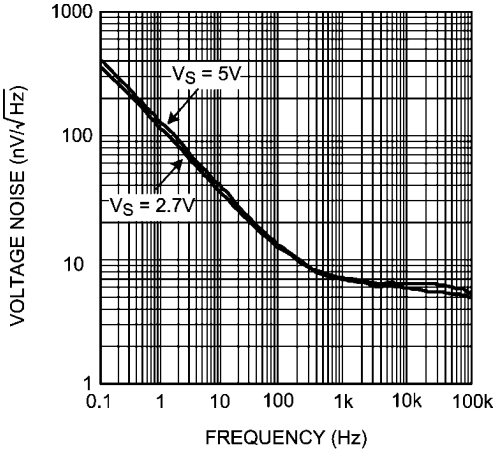
20204012

PSRR vs. Frequency



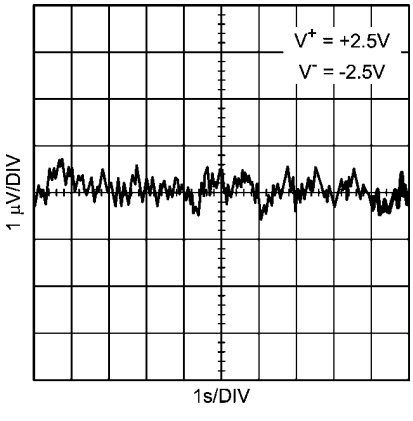
20204041

Input Referred Voltage Noise vs. Frequency



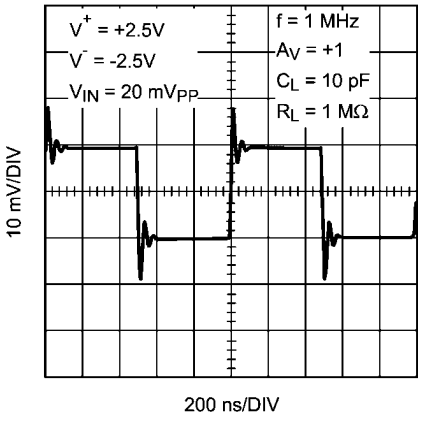
20204013

Time Domain Voltage Noise



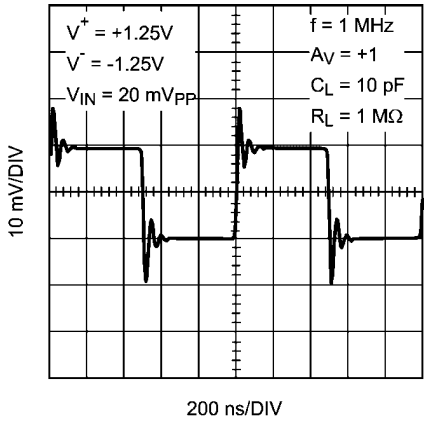
20204010

Small Signal Step Response



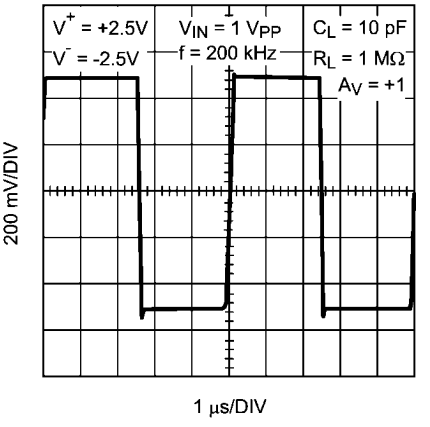
20204003

Small Signal Step Response



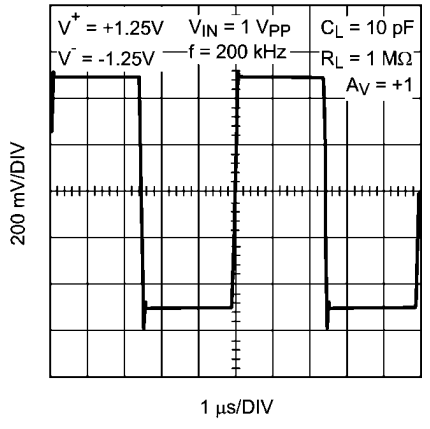
20204004

Large Signal Step Response



20204006

Large Signal Step Response



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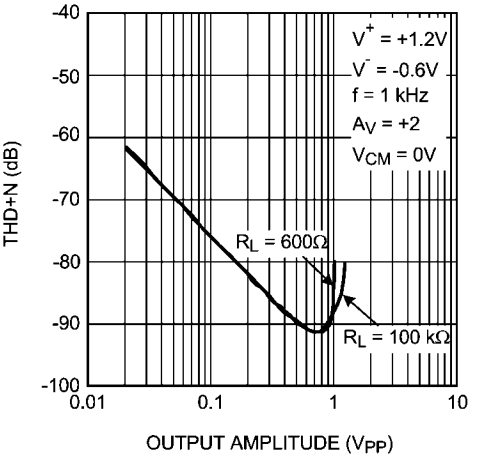
THD+N vs. Output Voltage



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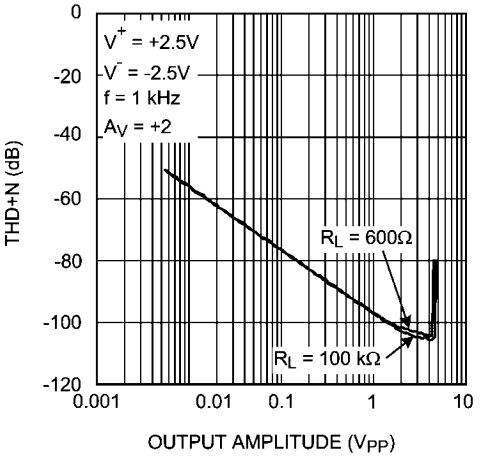
THD+N vs. Output Voltage



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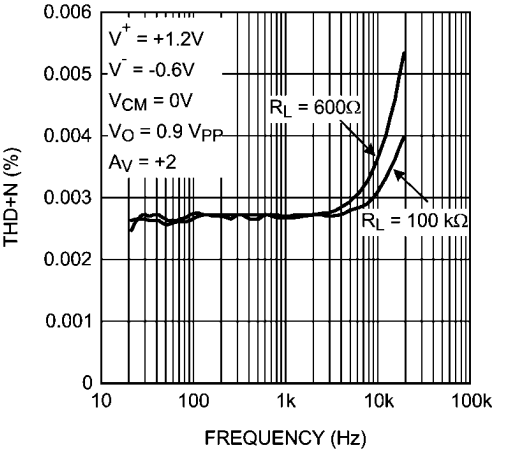
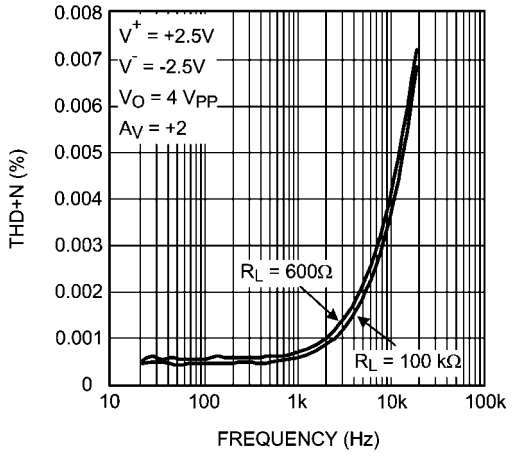
THD+N vs. Frequency



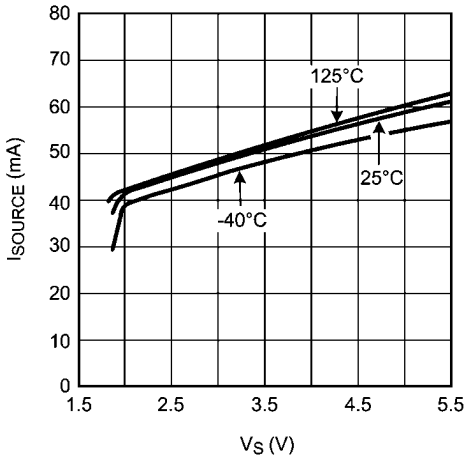
20204008

THD+N vs. Frequency



20204009

Sourcing Current vs. Supply Voltage



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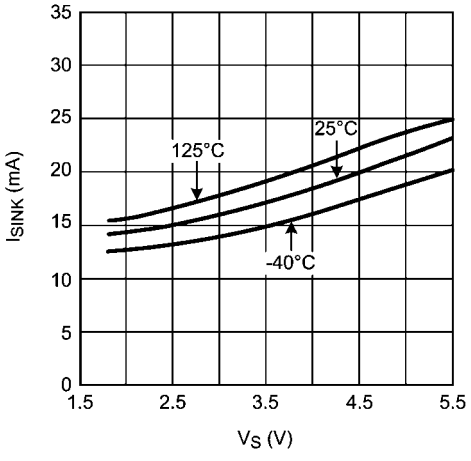
Sinking Current vs. Supply Voltage



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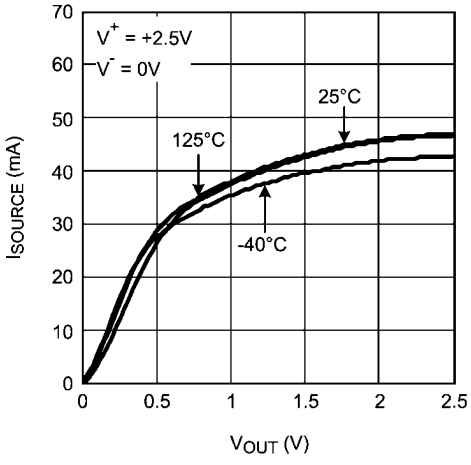
Sourcing Current vs. Output Voltage



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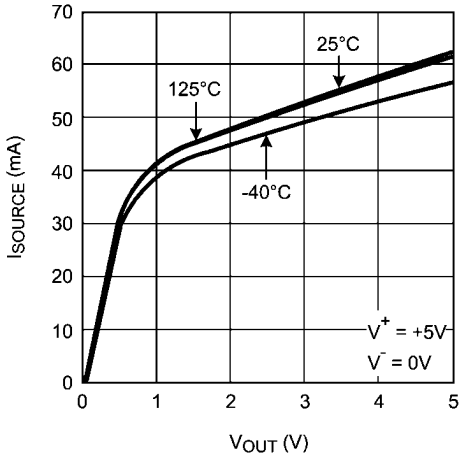

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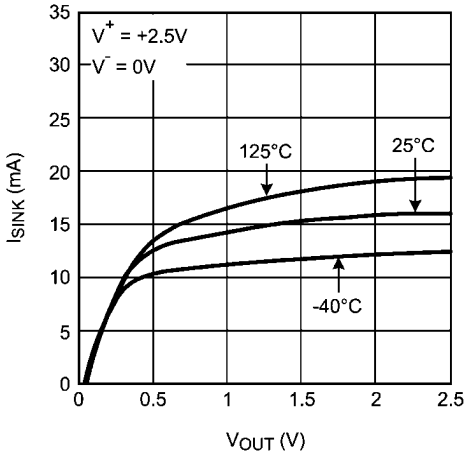

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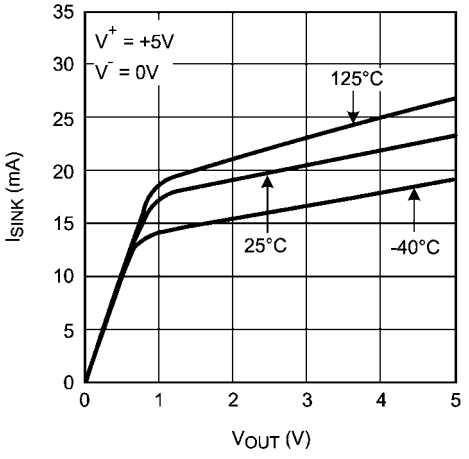
Sinking Current vs. Output Voltage



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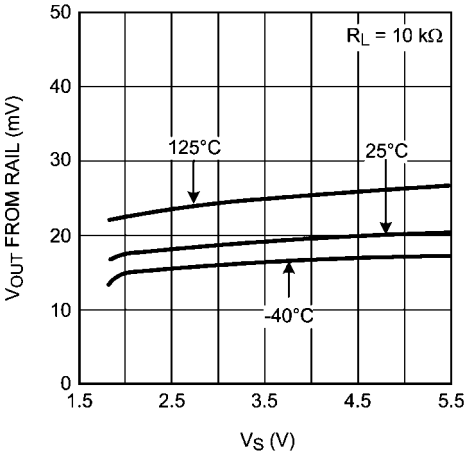
Output Swing High vs. Supply Voltage



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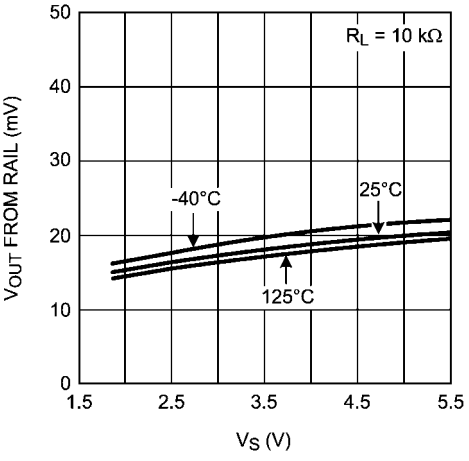
Output Swing Low vs. Supply Voltage



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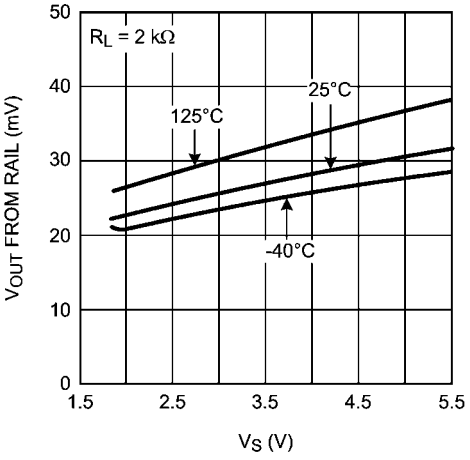
Output Swing High vs. Supply Voltage



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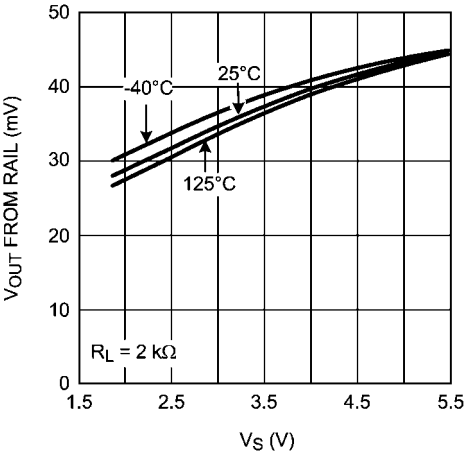
Output Swing Low vs. Supply Voltage



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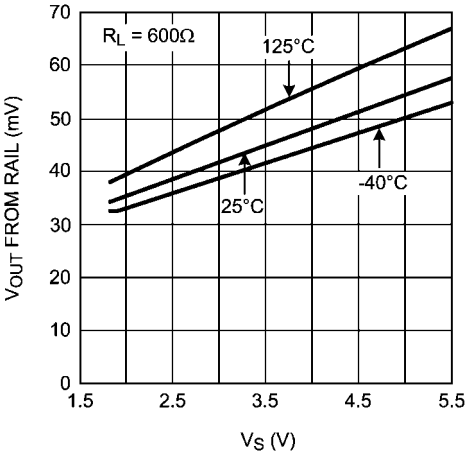
Output Swing High vs. Supply Voltage



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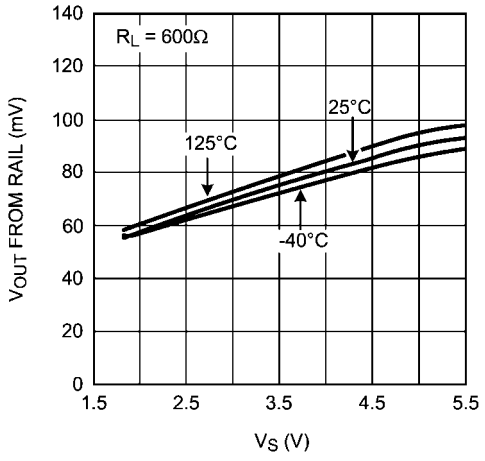
Output Swing Low vs. Supply Voltage



20204030

Application Information

ADVANTAGES OF THE LMP7721

Ultra Low Input Bias Current

The LMP7721 has the industry's lowest guaranteed input bias current. The ultra low input bias current is typically 3 fA, with a guaranteed limit of ±20 fA at 25°C, ±900 fA at 85°C and ±5 pA at 125°C when V_{CM} = 1V with a 5V or a 2.5V power supply.

Wide Bandwidth at Low Supply Current

The LMP7721 is a high performance amplifier that provides a 17 MHz unity gain bandwidth while drawing only 1.3 mA of current. This makes the LMP7721 ideal for wideband amplification in portable applications.

Low Input Referred Noise

The LMP7721 has a low input referred voltage noise density (6.5 nV/$\sqrt{Hz}$ at 1 kHz with 5V supply). Its MOS input stage ensures a very low input referred current noise density (0.01 pA/$\sqrt{Hz}$).

The low input referred noise and the ultra low input bias current make the LMP7721 stand out in maintaining signal fidelity. This quality makes the LMP7721 a suitable candidate for sensor based applications.

Low Supply Voltage

The LMP7721 has performance guaranteed at 2.5V and 5V power supplies. The LMP7721 is guaranteed to be functional at all supply voltages between 2.0V to 5.5V, for ambient temperatures ranging from −40°C to 125°C. This means that the LMP7721 has a long operational span over the battery's lifetime. The LMP7721 is also guaranteed to be functional at 1.8V supply voltage, for ambient temperatures ranging from 0°C to 125°C. This makes the LMP7721 ideal for use in low voltage commercial applications.

RRO and Ground Sensing

Rail-to-rail output swing provides the maximum possible output dynamic range. This is particularly important when operating at low supply voltages. An innovative positive feedback scheme is created to boost the LMP7721's output current drive capability. This allows the LMP7721 to source 30 mA to 40 mA of current at 1.8V power supply.

The LMP7721's input common mode range includes the negative supply rail which makes direct sensing at ground possible in single supply operation.

Unique Pinout

The LMP7721 has been designed with the IN+ and IN–, V^+ and V^- pins on opposite sides of the package. There are isolation pins between IN+ and V^-, IN– and V+. This unique pinout makes it easy to guard the LMP7721's input. This pinout design reduces the input bias current's dependence on common mode or supply bias.

The SOIC package features low leakage and it has large pin spacing. This lowers the probability of dust particles settling down between two pins thus reducing the resistance between the pins which can be a problem.

Input Protection

The LMP7721 input stage is protected from seeing excessive differential input voltage by a pair of back-to-back diodes attached between the inputs. This limits the differential voltage and hence prevents phase inversion as well as any performance drift. These diodes can conduct current when the input signal has a really fast edge, and, if necessary, should be isolated (using a resistor or a current follower) in such cases.

SYSTEM DESIGN TECHNIQUES WITH THE LMP7721

In order to take full advantage of the LMP7721's ultra low input bias current, a triaxial cable/connector is recommended when designing application systems.

A triaxial cable/connector is similar to a coaxial cable/connector and is often referred to as "triax". *Figure 1* shows the structure of the triax.

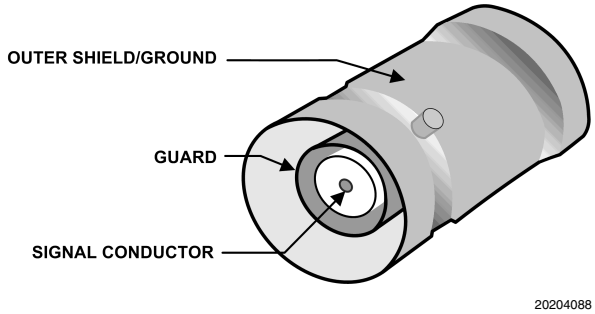


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FIGURE 1. The Structure of a Triax

The signal conductor and the guard of the triax should be kept at the same potential; therefore, the leakage current between them is practically zero. Since triax has an extra layer of insulation and a second conducting sheath, it offers greater rejection of interference than coaxial cable/connector.

TRANSIMPEDANCE AMPLIFIER EXAMPLE (INVERTING CONFIGURATION)

A transimpedance amplifier converts a small amount of current into voltage. The transfer function of a transimpedance amplifier is $V_{out} = -I_{in} * R_F$. *Figure 2* shows a typical transimpedance amplifier.

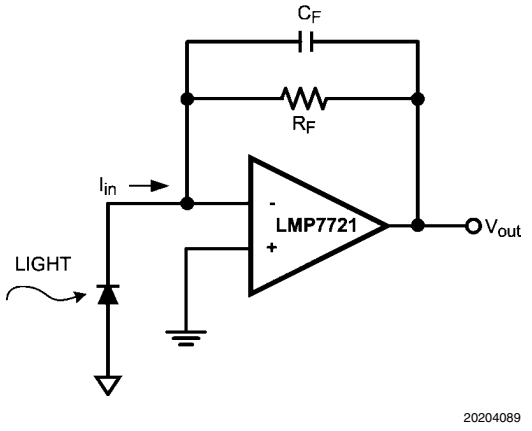


FIGURE 2. Photodiode Transimpedance Amplifier

The current is generated by a photodiode. The amount of the current is so small that it requires a large gain from the transimpedance amplifier in order to transform the miniscule current into easily detectable voltages. The larger the gain, the larger the value of R_F needed. When R_F is larger, the error caused by $I_{bias}*R_F$ increases. For example, if R_F is 1000 MΩ, and an op amp with 3 nA of I_{bias} is used, the $I_{bias}*R_F$ error at the output will be 3V! This error can be dramatically reduced to 3 µV by using the LMP7721.

Photodiodes are high impedance sensors which require careful design of the associated signal conditioning circuitry in order to meet the system challenges. CMOS input op amps are often used in transimpedance applications as they have extremely high input impedance. A triaxial cable is recommended for its very low noise pick-up.

A MOS input stage with ultra low input bias current, negligible input current noise, and low input voltage noise allows the LMP7721 to provide high fidelity amplification. In addition, the LMP7721 has a 17 MHz gain bandwidth product, which enables high gain at wide bandwidth. A rail-to-rail output swing at 5.5V power supply allows detection and amplification of a wide range of input currents. These properties make the LMP7721 ideal for transimpedance amplification.

Figure 3 is an example of the LMP7721 used as a transimpedance amplifier.

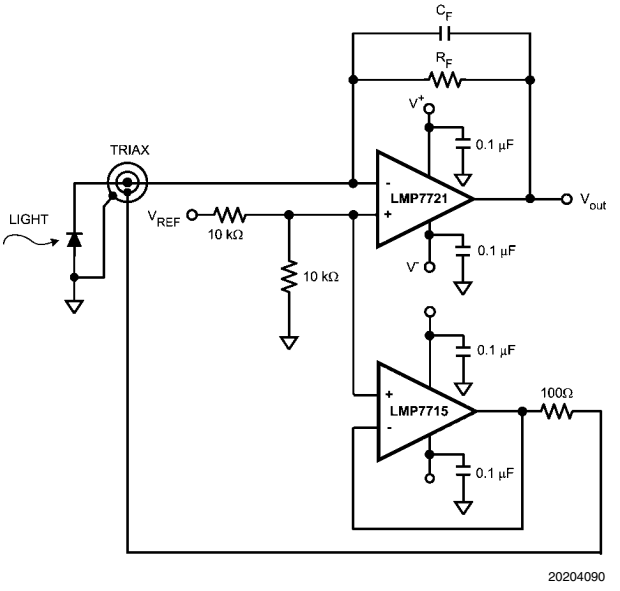


FIGURE 3. LMP7721 as Transimpedance Amplifier

The current generated by the photodiode is fed to the signal conductor of the triax and then sent to the inverting input of the LMP7721. The LMP7721's non-inverting input is biased at $V_{REF}/2$ for level shifting purposes. In this application, the non-inverting input is a low impedance node and hence is used to drive the LMP7715 which acts as a guard driver. The output of the guard driver is connected to the guard of the triax via a 100Ω isolation resistor. Ideally, the inverting and the non-inverting inputs of the amplifier are kept at the same potential through the operation of the amplifier. By connecting the signal conductor to the inverting input and letting the non-inverting input drive the guard, the signal conductor and the guard are kept at the same potential which prevents leakage from the signal source.

pH ELECTRODE AMPLIFIER EXAMPLE (NON-INVERTING CONFIGURATION)

The output of a pH electrode ranges from 415 mV to –415 mV as the pH changes from 0 to 14 at 25°C. The output impedance of a pH electrode is extremely high, ranging from 10 MΩ to 1000 MΩ. The ultra low input bias current of the LMP7721 allows the voltage error produced by the input bias current and electrode resistance to be minimal. For example, the output impedance of the pH electrode used is 10 MΩ, if an op amp with 3 nA of I_{bias} is used, the error caused due to this amplifier's input bias current and the source resistance of the pH electrode is 30 mV! This error can be greatly reduced to 30 nV by using the LMP7721.

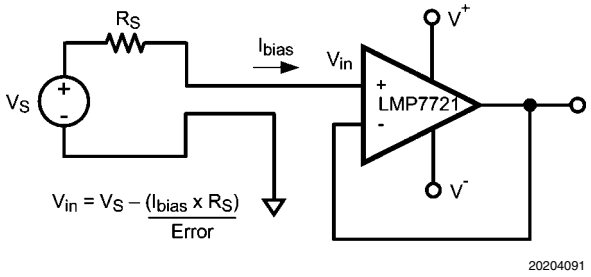


FIGURE 4. Error Caused by Amplifier's Input Bias Current and Sensor Source Impedance

Figure 5 is an example of the LMP7721 used as a pH sensor amplifier.

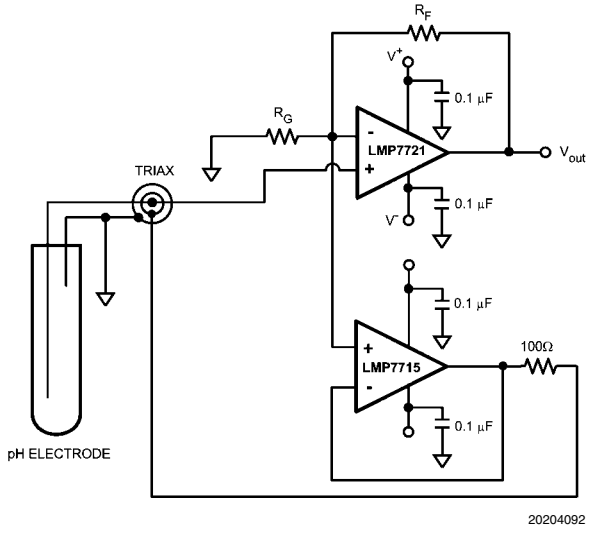


FIGURE 5. LMP7721 as pH Electrode Amplifier

The output voltage from the pH electrode is fed to the signal conductor of the triax and then sent to the non-inverting input of the LMP7721. In this application, the inverting input is a low impedance node and hence is used to drive the LMP7715 which acts as a guard driver. The output of the guard driver is connected to the guard of the triax via a 100Ω isolation resistor. Ideally, the inverting and the non-inverting inputs of the amplifier are kept at the same potential through the operation of the amplifier. By connecting the signal conductor to the non-inverting input and letting the inverting input drive the guard, the signal conductor and the guard are kept at the same potential which prevents leakage from the signal source.

LAYOUT AND ASSEMBLY CONSIDERATIONS

In order to capitalize on the LMP7721's ultra low input bias current, careful circuit layout and assembly are required. Guarding techniques are highly recommended to reduce parasitic leakage current by isolating the LMP7721's input from large voltage gradients across the PC board. A guard is a low impedance conductor that surrounds an input line and its potential is raised to the input line's voltage. The input pins should be fully guarded as shown in *Figure 6*. The guard traces should completely encircle the input connections. In addition, they should be located on both sides of the PCB and be connected together.

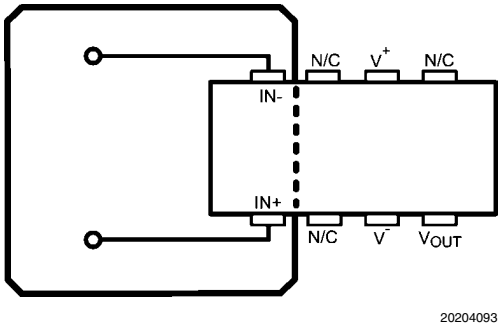
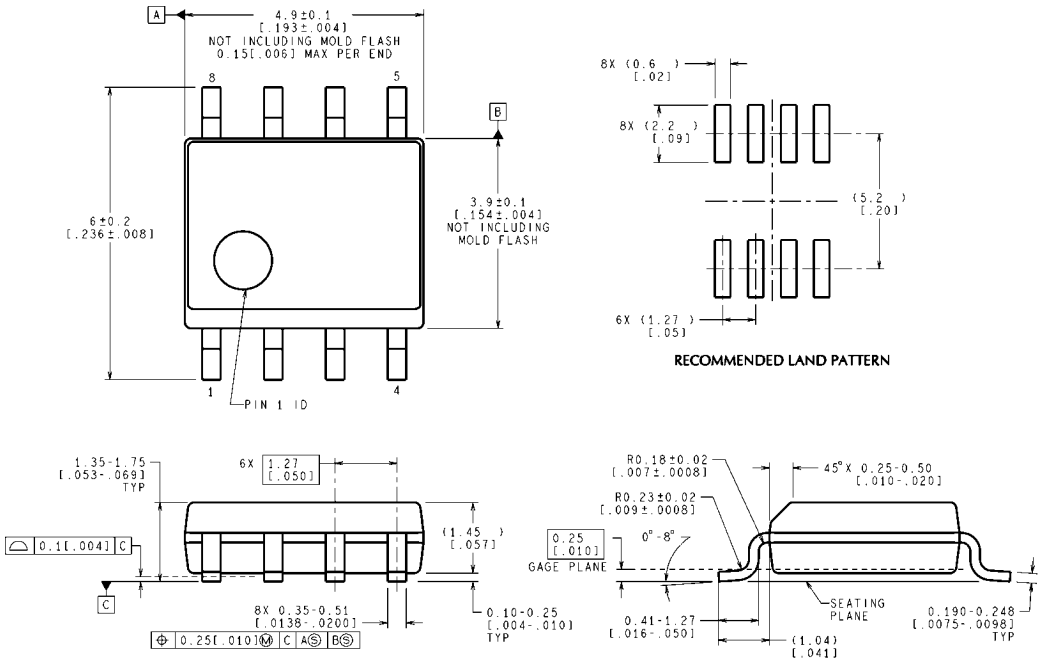


FIGURE 6. Circuit Board Guard Layout

Solder mask should not cover the input and the guard area including guard traces on either side of the PCB.

Sockets are not recommended as they can be a significant leakage source. After assembly, a thorough cleaning using commercial solvent is necessary.

Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
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M08A (Rev L)

8-Pin SOIC
NS Package Number M08A

Notes

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